everyday genius

MT3620

Product Brief

Version: 1.5
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Document Revision History

Revision	Date	Description
1.0	12 October 2017	Initial customer release.
1.1	4 April 2018	Additional information added.
1.2	18 November 2018	Section 4 added.
1.3	9 September 2019	1. Removed electrical/ pin info, which is already listed in datasheet 2. Add RoHS compliant
1.4	6 April 2020	Remove IEEE 802.11 a/ k/ r
1.5	11 May 2020	1. Update top mark 2. Fix document reference 3. Add ordering contact information

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1.   System Overview

1.1   General Description

MT3620 is a highly integrated single chip tri-core MCU designed to meet the requirements of modern, robust internet-connected devices. It leverages the Microsoft Azure Sphere security architecture to provide an unprecedented level of security to connected device manufacturers. For the lifetime of the device the Azure Sphere system provides device authentication and attestation, supports remote over-the-air software updates to maintain security in the face of evolving attacks, and automates error logging and reporting. Please refer to the "Azure Sphere Platform Overview" document from Microsoft for more information.

MT3620 features an application processor subsystem based on an ARM Cortex-A7 core which runs at up to 500MHz. The chip also includes two general purpose ARM Cortex-M4F I/O subsystems, each of which runs at up to 200MHz. These subsystems were designed to support real-time requirements when interfacing with a variety of on-chip peripherals including UART, I2C, SPI, I2S, and ADC. They are completely general-purpose Cortex-M4F units which may be tailored to specific application requirements. On-chip peripherals may be mapped to any of the three end-user accessible cores, including the CA7.

In addition to these three end-user accessible cores, MT3620 contains a security subsystem with its own dedicated CM4F core for secure boot and secure system operation. There is also a Wi-Fi subsystem controlled by a dedicated N9 32-bit RISC core. This contains a 1x1 dual-band 802.11a/b/g/n radio, baseband and MAC designed to support both low power and high throughput applications without placing computational load on the user-accessible cores.

MT3620 also includes over 5MB of embedded RAM, split among the various cores. There is a fully-integrated PMU and a real-time clock. Flash memory is integrated in the MT3620 package. Please refer to the "Azure Sphere MT3620 Support Status" document from Microsoft for information about how much memory and which hardware features are available to end-user applications. Only hardware features supported by the Azure Sphere system are available to MT3620 end-users.

1.2   Main Features

1.2.1   Platform

- ARM Cortex A7 with NEON and FPU support and 64kB L1 instruction cache, 32kB L1 data cache, 256kB L2 cache, and 4MB system memory for the Azure Sphere operating system and user applications; ideal for high-level user code
- Two general purpose ARM Cortex M4 cores, each with 192kB TCM, 64kB SRAM, and integrated FPU; ideal for real-time control requirements
- In-package serial flash
- User-accessible cores support execute-in-place (XIP) from flash
- Five "ISU" serial interface blocks which can be configured as I2C master. I2C slave, SPI master, SPI slave, or UART; I2C runs at up to 1MHz, SPI at up to 40MHz, and UARTs at up to 3Mbps
- Two I2S interfaces supporting slave and TDM slave modes
- Eight-channel, 12-bit, 2MS/s single-ended successive approximation ADC using internal 2.5V or external 1.8V reference
- 76 programmable GPIO pins with programmable drive strength (some multiplexed with other functions)
- 12 PWM outputs
- 24 external interrupt inputs
- Six hardware counter blocks which can count and measure pulses and perform quadrature decoding

- RTC can run from dedicated 32 kHz external input, from on-die 32 kHz oscillator, from on-die ring oscillator, or from main oscillator
- One-time programmable e-fuse block for storing chip-specific information
- Two additional, dedicated UARTs, one for each CM4F I/O subsystem
- Per-core watchdog timers
- Per-core general-purpose timers

1.2.2   Pluton Security Subsystem

- Provides security and secure power management for entire chip
- Dedicated ARM Cortex-M4F security processor with 128kB secured TCM and 64kB secured mask ROM bootloader
- Microsoft Azure Sphere Pluton security engine provides cryptographic engines and hardware root of trust
- Hardware random number generator with entropy monitoring system to ensure true random numbers
- Side-channel attack and tampering counter-measures
- Dedicated, secure one-time programmable e-fuse block for storing security-related configuration information
- Provides secure boot via ECDSA, hardware support for remote attestation and certificate-based security

1.2.3   Wi-Fi

- Dedicated high-performance N9 32-bit RISC core
- Dedicated one-time programmable e-fuse block for storing Wi-Fi specific calibration and configuration information
- IEEE 802.11 b/g/n compliant
- Supports 20MHz bandwidth in 2.4GHz band and 5GHz band
- Dual-band 1T1R mode
- Supports STBC, LDPC, explicit beamforming as the beamformee
- Greenfield, mixed mode, legacy modes support

- IEEE 802.11 d/e/h/i/w support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Built-in RX diversity support
- Full TX/RX antenna diversity support via external DPDT switch
- Optional external LNA and PA support
- Multiple external support component configuration options for BoM flexibility

1.2.4   Power Management and Clock Sources

- Integrated high efficiency power management unit with single 3.3V power supply input
- Integrated under-voltage lockout, three low drop-out (LDO) regulators and a high efficiency buck converter
- Integrated comparator for supply brown-out detection with configurable threshold
- 20/40/26/52MHz crystal clock support with low power operation mode
- 32kHz crystal real-time clock with external battery-backup supply

1.2.5   Management Interfaces

- 'Recovery' UART for re-loading device firmware
- 'Service' UART for in-production and in-field firmware update and device management

1.2.6   Technology and Package

- Highly integrated 40nm RFCMOS technology
- System-in-package (SIP) serial flash
- 12mm x 12mm 164 pin DR-QFN package
- Designed to support 4-layer PCB construction based on widely supported PCB design rules
- RoHS compliant
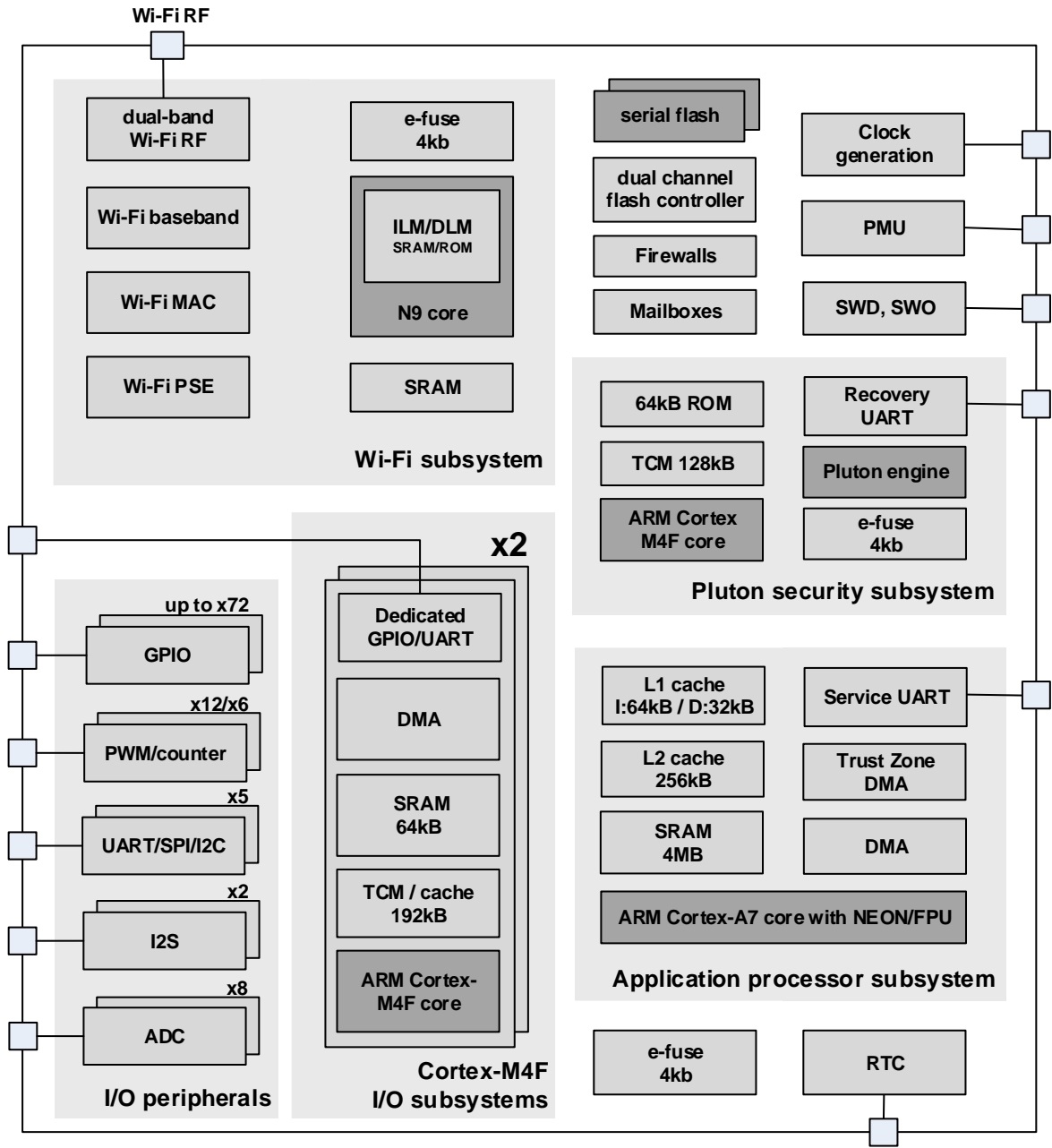
1.3   MT3620 Block Diagram

Wi-Fi RF

dual-band Wi-Fi RF

Wi-Fi baseband

Wi-Fi MAC

Wi-Fi PSE

e-fuse 4kb

ILM/DLM SRAM/ROM

N9 core

SRAM

Wi-Fi subsystem

serial flash

dual channel flash controller

Firewalls

Mailboxes

Clock generation

PMU

SWD, SWO

64kB ROM

TCM 128kB

ARM Cortex M4F core

Recovery UART

Pluton engine

e-fuse 4kb

Pluton security subsystem

up to x72

GPIO

x12/x6

PWM/counter

x5

UART/SPI/I2C

x2

I2S

x8

ADC

I/O peripherals

x2

Dedicated GPIO/UART

DMA

SRAM 64kB

TCM / cache 192kB

ARM Cortex-M4F core

Cortex-M4F I/O subsystems

L1 cache I:64kB / D:32kB

L2 cache 256kB

SRAM 4MB

ARM Cortex-A7 core with NEON/FPU

Service UART

Trust Zone DMA

DMA

Application processor subsystem

e-fuse 4kb

RTC

Figure 1. MT3620 Block Diagram

2.   Ordering information

Part number	Total flash	Flash configuration
MT3620AN	16MB	2x 8MB dual channel quad SPI

For further ordering information, please contact: https://www.mediatek.com/about/contact-us

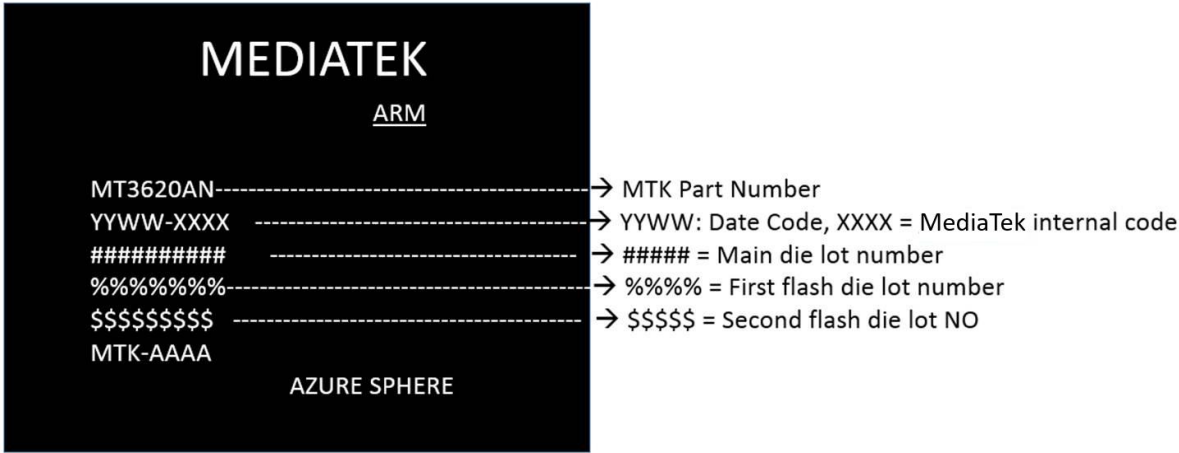# 3.   Packaging and Thermal Information

3.1   Top Mark

Figure 2. Top Mark

3.2   Thermal Characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Ψ_{Jt} assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Ψ_{Jt} to estimate the junction temperature.

Table 1. Thermal Characteristics

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum junction temperature (plastic package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	40	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	17.07	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	12.56	°C/W

Note:
[1] JEDEC 51-9 system FR4 PCB size: 101.5mm x 114.3mm
[2] 10.4mm x 10.4mm BGA package

4. General

Please make sure to use the most recently issued product brief before initiating or completing a design. Customers are responsible for the design, operation, suitability and fitness for intended use of their own and customer's third-party customers' applications and products using MediaTek's products. By use of MediaTek's product, customer acknowledges and agrees to have in place appropriate and sufficient system and precaution measures and conduct all necessary testing and modification to minimize risks relating to customer's use of MediaTek's product within customer's product and application. Except as otherwise explicitly provided in the written agreement between MediaTek and customer, MediaTek makes no other warranties with respect to MediaTek's products to customer, expressed, implied, statutory or otherwise, and MediaTek disclaims any implied warranty, including without limitation any implied warranty of merchantability, non-infringement of third party intellectual property right, or fitness for a particular purpose.