



*everyday genius*

# **MediaTek MT3620**

## **Secure Wireless Connectivity Chip**

### **Hardware User Guide**

Version: v2.2  
Release Date: 2021-01-26

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## 1 Document Revision History

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Version	Date	Change List
V2.0	2020/02/19	1 <sup>st</sup> public release.
V2.1	2020/05/11	Update top marking.
V2.2	2021/01/26	Remove “Code-name 4x4” Remove “Mt. Blanca”

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## 5 System overview

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### 5.1 General Description

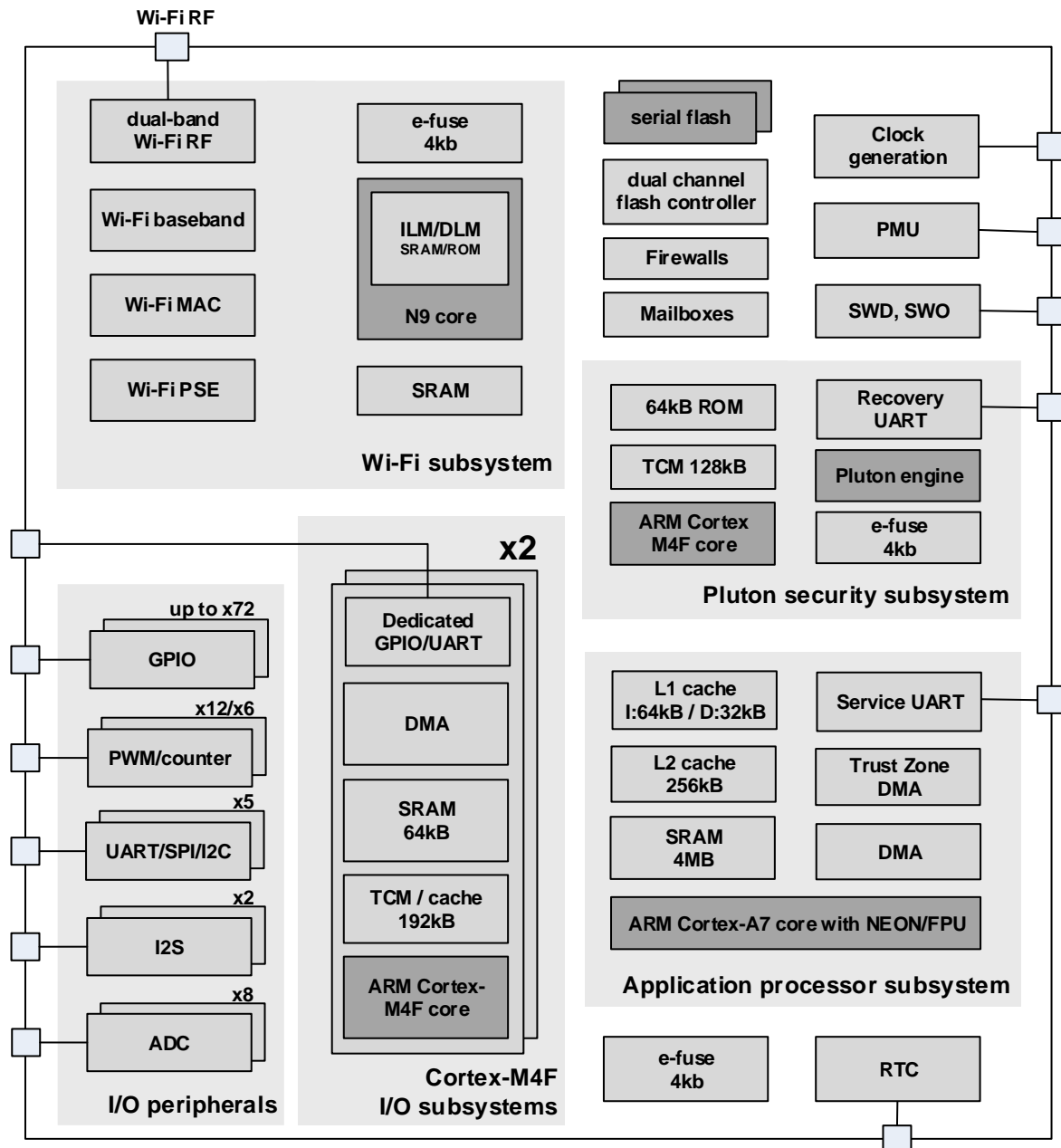
MT3620 is a highly integrated single chip tri-core MCU designed to meet the requirements of modern, robust internet-connected devices. It leverages the Microsoft Azure Sphere security architecture to provide an unprecedented level of security to connected device manufacturers. For the lifetime of the device the Azure Sphere system provides device authentication and attestation, supports remote over-the-air software updates to maintain security in the face of evolving attacks, and automates error logging and reporting. Please refer to the “Azure Sphere Platform Overview” document from Microsoft for more information.

MT3620 features an application processor subsystem based on an ARM Cortex-A7 core which runs at up to 500MHz. The chip also includes two general purpose ARM Cortex-M4F I/O subsystems, each of which runs at up to 200MHz. These subsystems were designed to support real-time requirements when interfacing with a variety of on-chip peripherals including UART, I2C, SPI, I2S, and ADC. They are completely general-purpose Cortex-M4F units which may be tailored to specific application requirements. On-chip peripherals may be mapped to any of the three end-user accessible cores, including the CA7.

In addition to these three end-user accessible cores, MT3620 contains a security subsystem with its own dedicated CM4F core for secure boot and secure system operation. There is also a Wi-Fi subsystem controlled by a dedicated N9 32-bit RISC core. This contains a 1x1 dual-band 802.11b/g/n radio, baseband and MAC designed to support both low power and high throughput applications without placing computational load on the user-accessible cores.

MT3620 also includes over 5MB of embedded RAM, split among the various cores. There is a fully-integrated PMU and a real-time clock. Flash memory is integrated in the MT3620 package. Please refer to the “Azure Sphere MT3620 Support Status” document from Microsoft for information about how much memory and which hardware features are available to end-user applications. Only hardware features supported by the Azure Sphere system are available to MT3620 end-users.

## 5.2 Block Diagram



**Figure 5-1 MT3620 Block Diagram**



## 6 PCB Stack Up and Impedance Control

### 6.1 PCB Stack-up

The PCB stack-up should include a closely-spaced power and ground plane pair; a 4 layer PCB stack-up is recommended, as shown in Table 1-1. Table 1-2 shows the recommended structure of the 4 layer PCB.

**Table 6-1. PCB Single Setting**

4 Layer PCB Single Setting
<ul style="list-style-type: none"> <li>• <b>Layer-1: signal</b></li> <li>• <b>Layer-2: ground plane, unbroken</b></li> <li>• <b>Layer-3: Vdd (3.3V) plane</b></li> <li>• <b>Layer-4: signal</b></li> </ul>

**Table 6-2. PCB Layer Stack-up**

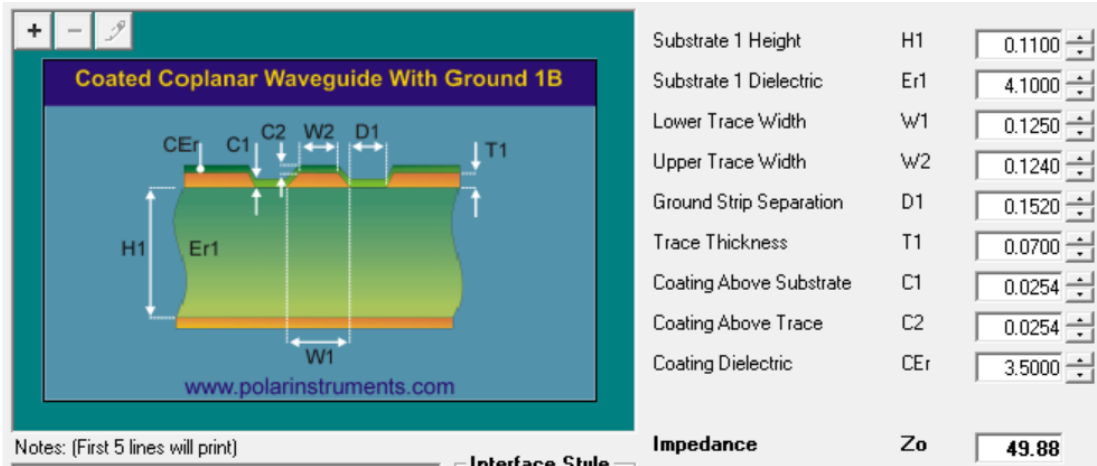
PCB Stack Up					
Layer	Signal Type	Layer Type	PCB thickness		$\epsilon_r$
			mils	mm	
Top side solder mask			1.0	0.025	3.5
Layer-1	differential & signal	copper + plating	2.76	0.07	
		prepreg	4.33	0.11	4.1
Layer-2	GND	copper	1.38	0.035	
		core	47.24	1.2	4.4
Layer-3	Vdd/GND	copper	1.38	0.035	
		prepreg	4.33	0.11	4.1
Layer-4	differential & signal	copper + plating	2.76	0.07	
Bottom side solder mask			1.0	0.025	3.5
TOTAL			66.18 (mils)	1.68 (mm)	

Select dielectric thickness to support required characteristic signal trace impedances and power plane capacitance and inductance. Perform resonance analysis on all plane cavities.

## 6.2 Transmission Line

### 6.2.1 50Ω Single-ended

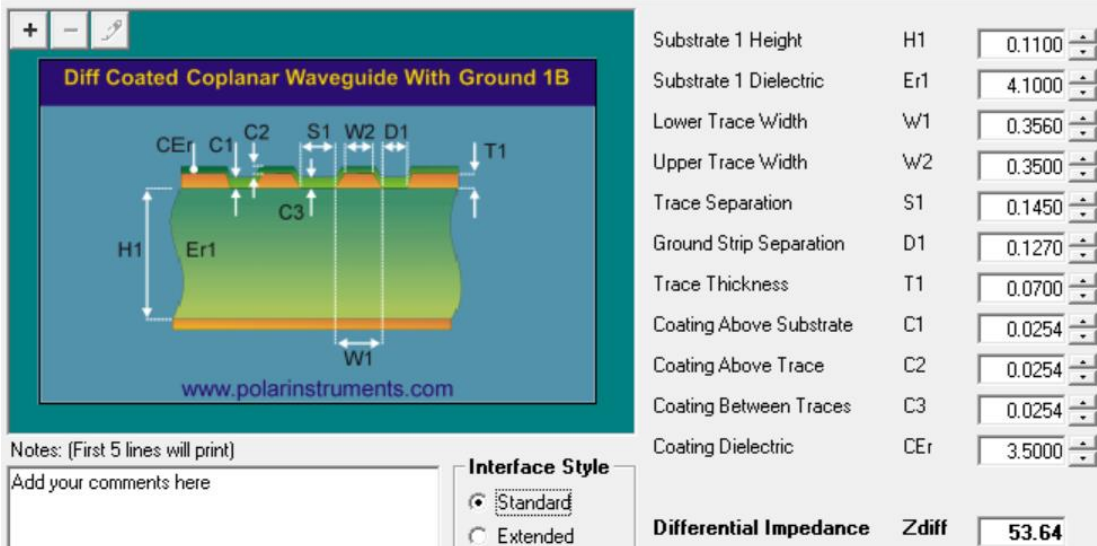
50Ω single-ended transmission line on the top plane is in reference to the GND plane on layer-2.



**Figure 6-1. A 50Ω single-ended transmission line in reference to Layer-2**

### 6.2.2 50Ω Differential-ended

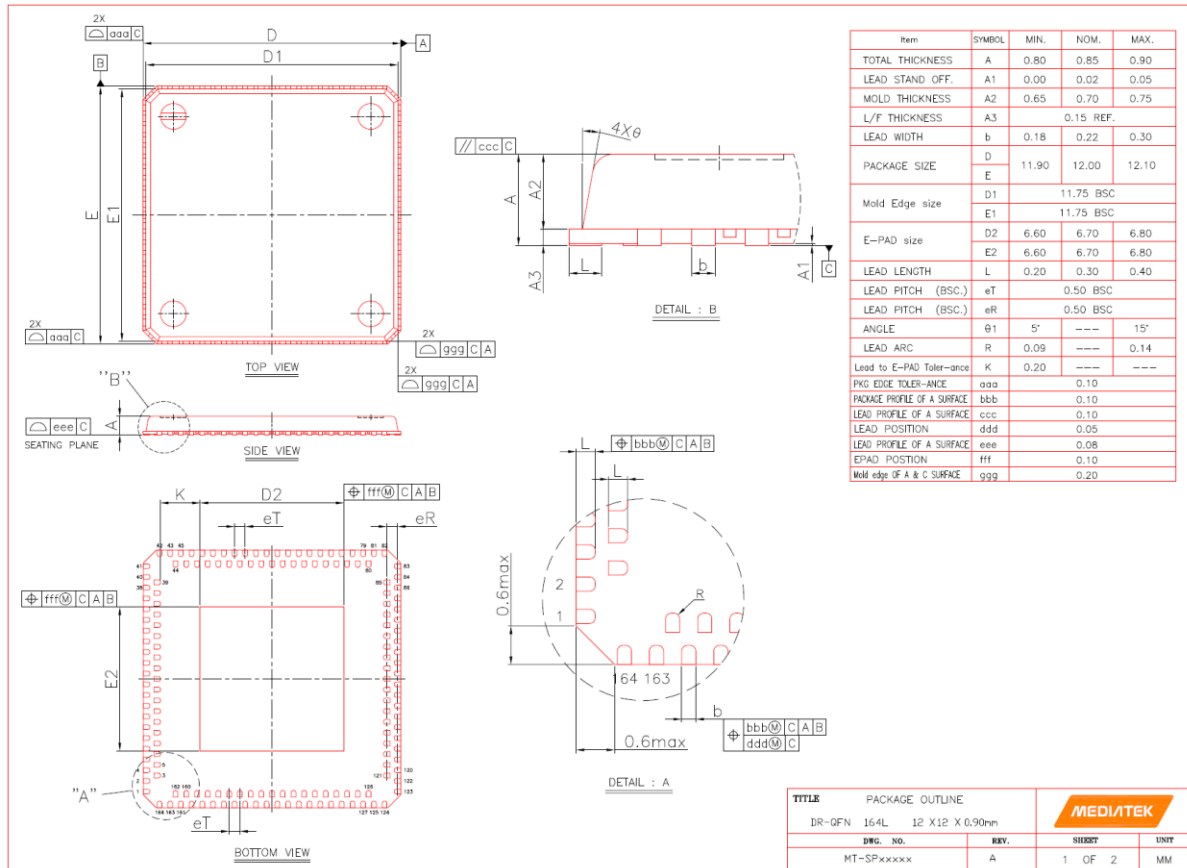
50Ω differential transmission line on the top plane is in reference to the GND plane on layer-2.



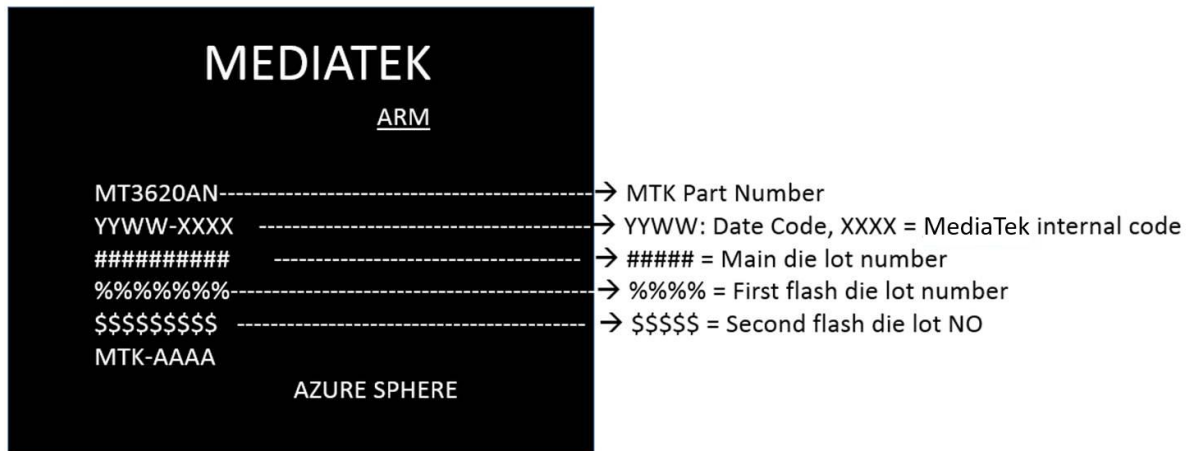
**Figure 6-2. A 50Ω differential transmission line in reference to Layer-2**

Impedance matching should be guaranteed by the PCB manufacturer.

## 6.3 Package Information



## 6.4 Top Marking



## 7 RF Front-End Circuit Design

### 7.1 RF System Overview

The following circuit schematics show two possible RF configurations. The first supports dual band (5GHz and 2.4GHz) and includes support to transmit and receive diversity. The second circuit is a simplified version that supports single band (2.4GHz) and a single antenna (no diversity).

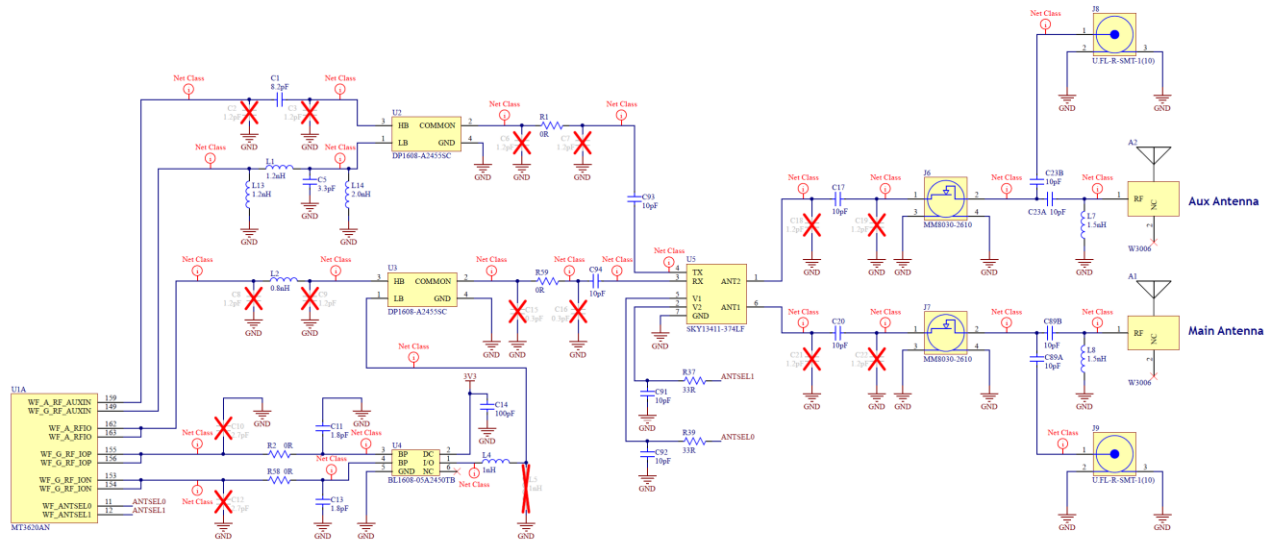


Figure 7-1 RF circuit supporting 5G/2.4G, with full transmit/receive diversity

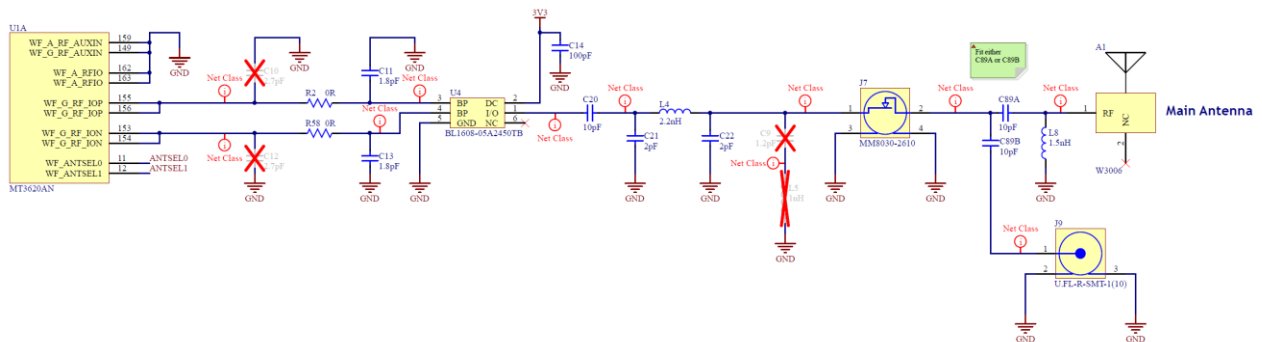


Figure 7-2 RF circuit supporting 2.4G, single antenna (no diversity)

### 7.2 Wi-Fi RF Main Path Schematic

#### WF\_A\_RFIO:

- WF\_A\_RFIO is the single-ended input and output interface for the 5GHz Wi-Fi radio transceiver.
- The 5GHz Wi-Fi transceiver radio integrates a balun, PA, LNA and T/R switch.

#### WF\_G\_RF\_IOP and WF\_G\_RF\_ION:

- WF\_G\_RF\_IOP and WF\_G\_RF\_ION form the differential input and output interface of the 2.4GHz Wi-Fi radio transceiver.
- The 2.4GHz Wi-Fi transceiver integrates a PA, LNA and T/R switch.
- The differential pair is 50Ω having a matching network between 50Ω-50Ω balun.

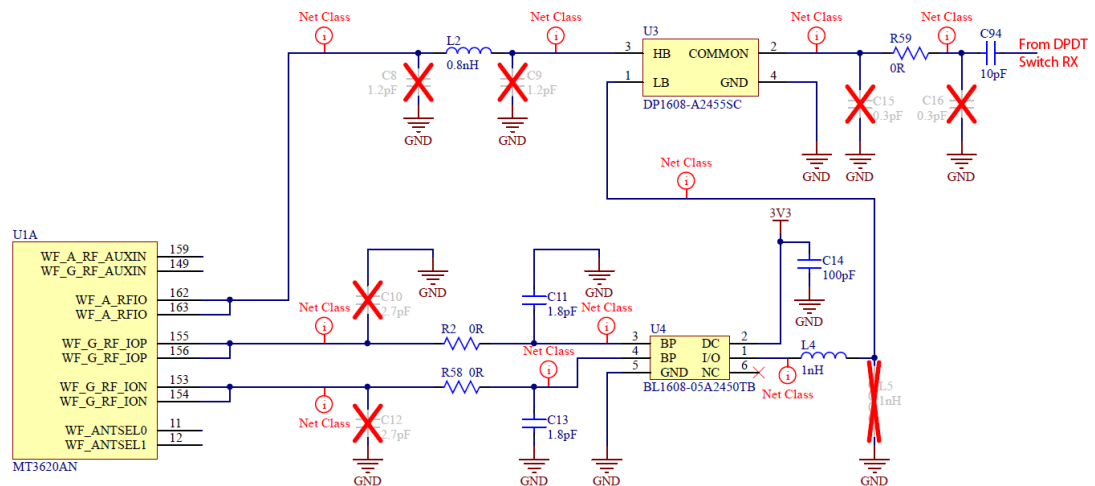


Figure 7-3 RF 5G/2.4G Main Path Circuit

### 7.3 Wi-Fi RF Auxiliary Path Front-End Schematic

#### WF\_A\_RF\_AUXIN:

- WF\_A\_RF\_AUXIN is an additional single-ended input interface of the 5GHz Wi-Fi receiver which support a 5GHz receive diversity function.

#### WF\_G\_RF\_AUXIN:

- WF\_G\_RF\_AUXIN is an additional single-ended input interface of the 2.4GHz Wi-Fi receiver which supports a 2.4GHz receive diversity function.

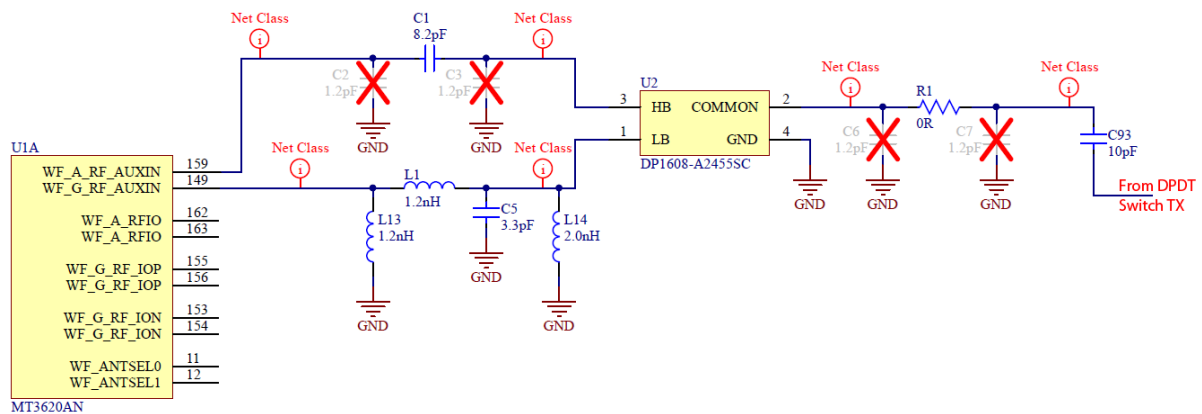


Figure 7-4 RF Auxiliary Path Circuit

## 7.4 RF Component Placement

### 7.4.1 RF matching circuit placement

#### 2.4GHz matching component placement

- Please make placement and layout of 2GHz matching network according to the following figures.

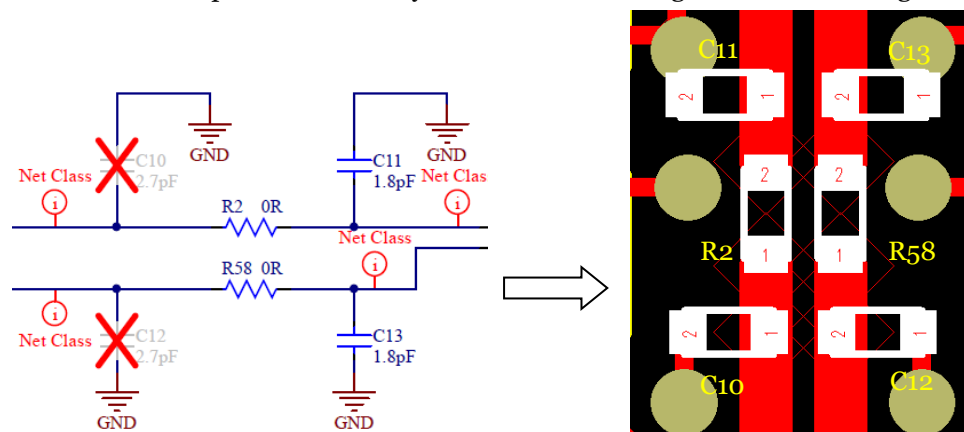
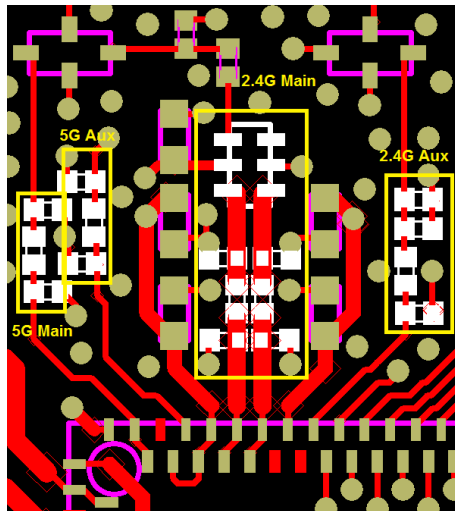


Figure 7-5 Matching Components Layout Placement

- We strongly recommend you place RF matching circuits, including the main 2.4GHz, main 5GHz and auxiliary 5GHz paths, near the MT3620 chip as the figure shows below.

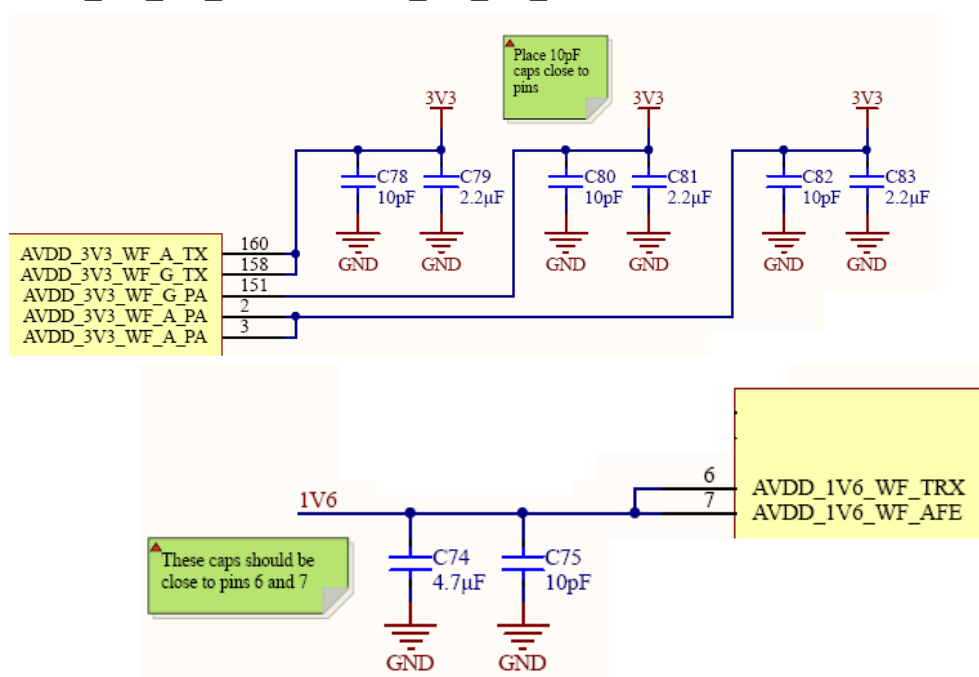


**Figure 7-6 Layout Placement for 2.4GHz/5GHz Matching Circuits**

#### 7.4.2 RF Power circuit placement

There are two RF power rails which can share capacitors, shown in Figure 7-5

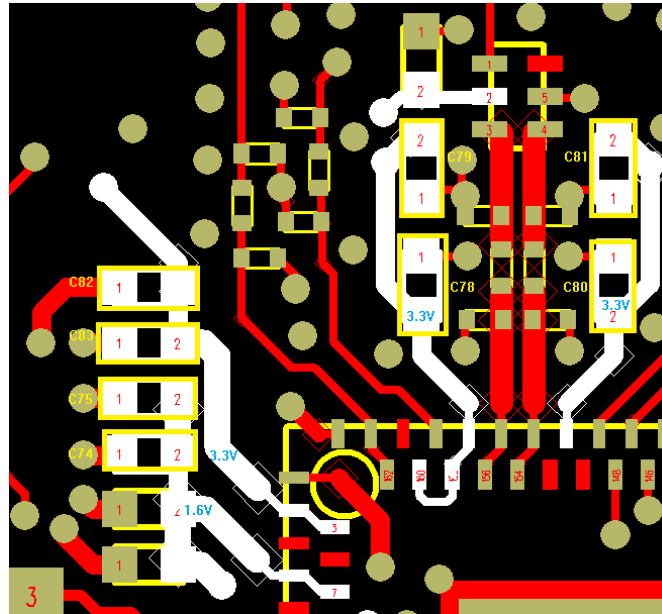
1. AVDD\_3V3\_WF\_A\_TX, AVDD\_3V3\_WF\_G\_TX, AVDD\_3V3\_WF\_G\_PA and AVDD\_3V3\_WF\_A\_PA
2. AVDD\_1V6\_WF\_TRX and AVDD\_1V6\_WF\_AFE



**Figure 7-7 RF Power Rails**

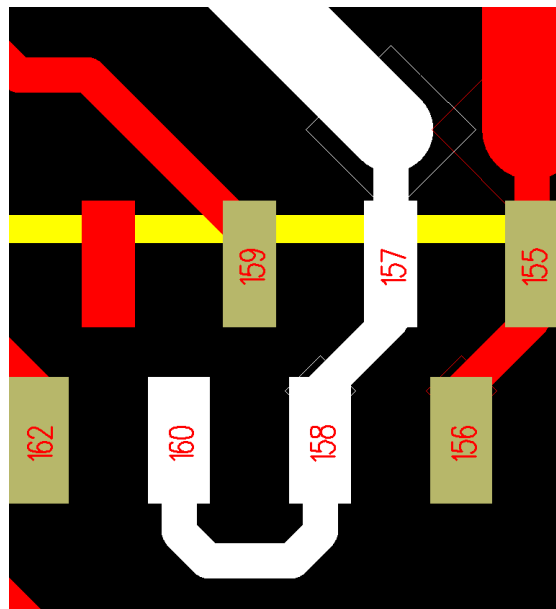


Place these RF power capacitors as close as possible to the relevant pins. Each pin/pin-pair should be decoupled with a 2.2uF or 4.7uF capacitor in parallel with a 10pF capacitor. The 10pF capacitor effectively acts as a filter to reduce high-frequency noise.



**Figure 7-8 RF Power Supply Capacitor Placement**

If necessary, pin 157 (NC) can be used for AVDD\_3V3\_WF\_A\_TX trace routing as shown below.



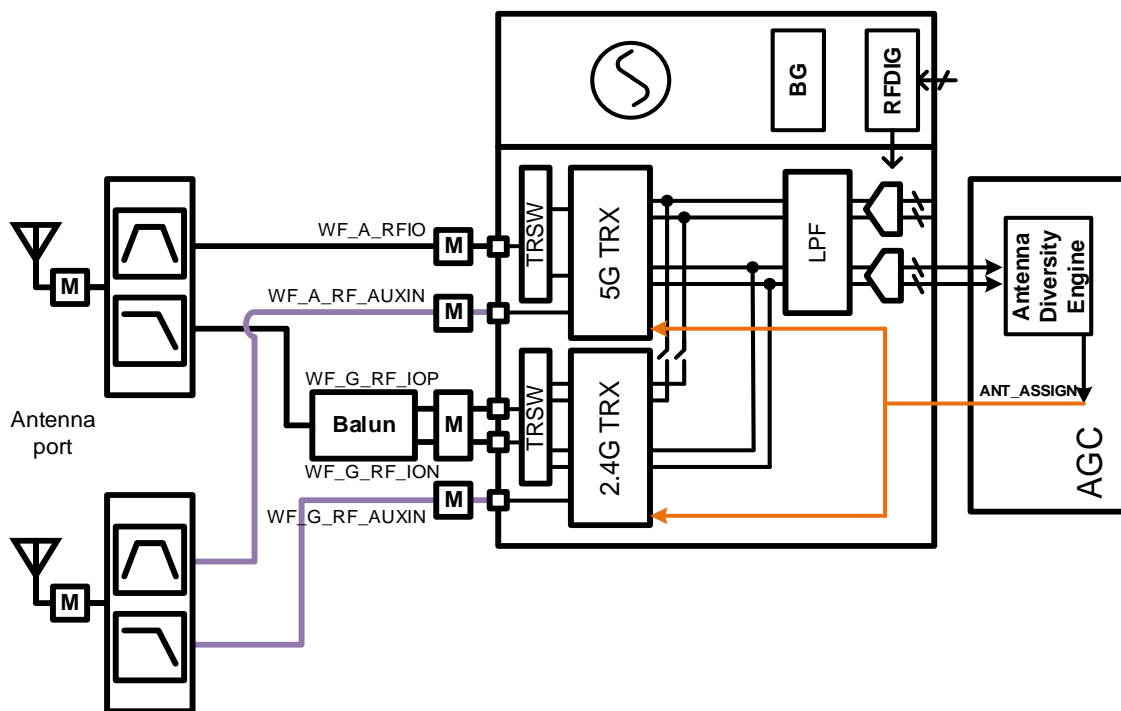
**Figure 7-9 AVDD\_3V3\_WF\_A\_TX Trace Routing Method**

## 7.5 Diversity

### 7.5.1 Receive diversity is supported in hardware

The figure shown below is a block diagram of the RF front-end design when using on-chip receive diversity.

- Receive diversity is supported without the need for an external switch, by way of two additional receive-only diversity antenna ports.
- Per-packet antenna diversity (fast-diversity).
- Baseband software automatically controls switching between the main and auxiliary receive paths.
- Transmission only occurs through the main antenna port.

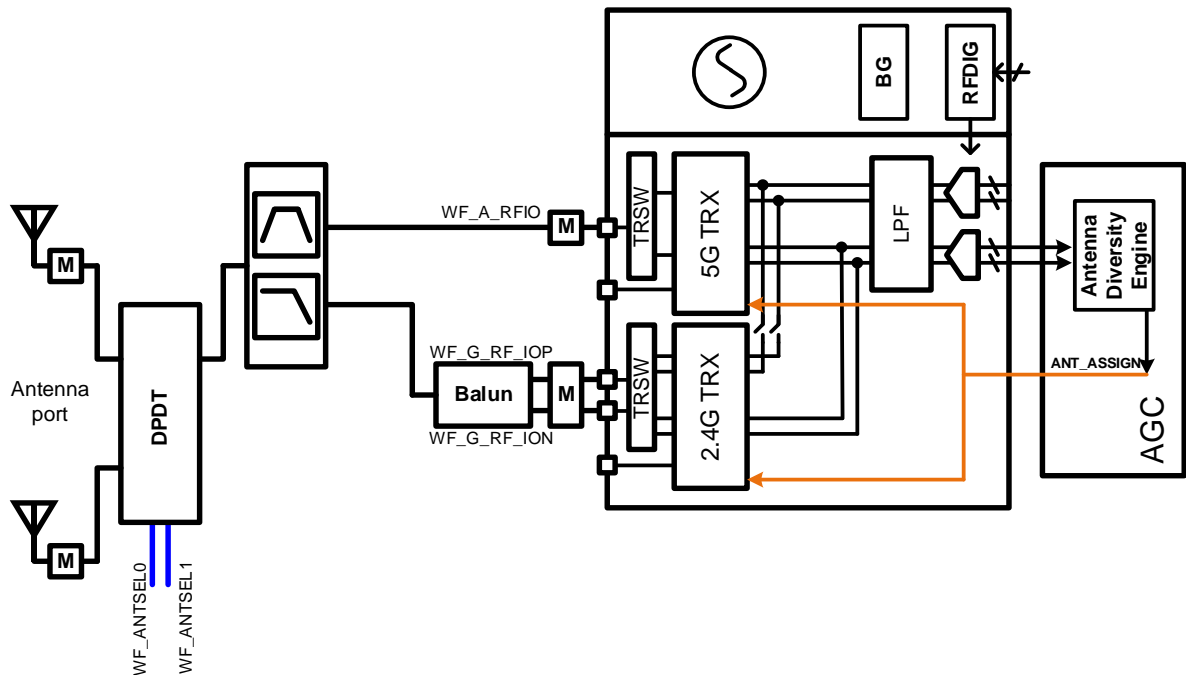


### 7.5.2 Full transmit/receive diversity is supported in software but requires an external DPTP switch

The figure shown below shows the RF front-end design when supporting full transmit/receive antenna diversity.

- Full transmit/receive antenna diversity requires an external DPDT RF switch.
- In this case RF transceiving is fixed to the main path only, and does not use the auxiliary diversity receive ports.

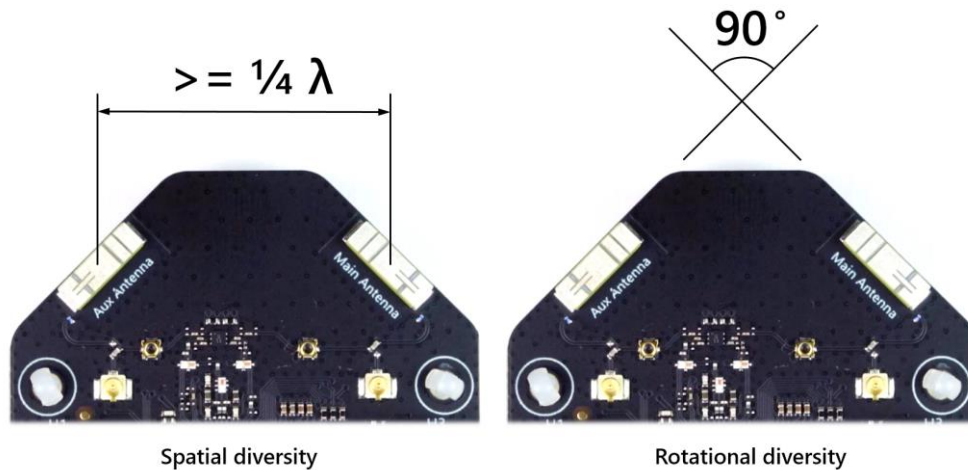
- If full diversity is selected, the baseband software automatically drives the WF\_ANTSEL0/1 pins to control the external diversity switch.



### 7.5.3 Antenna Placement Guidelines for Antenna Diversity

Radio signals rarely pass directly from one point in space to another. In reality, the signals are reflected off walls etc. and will form multiple simultaneous paths between the two points. This results in points in space where there are strong signals, and conversely, points where there are very weak signal, or nulls. In the case of a device having a single antenna, if the antenna happens to be in a null, it may struggle or even fail to reliably connect and transfer data.

Adopting the use of two antenna can help to overcome these problems. More specifically though, to gain the full advantages of antenna diversity the two antennas need to be (a) physically separated by a distance of at least a  $\frac{1}{4}$  wavelength. At 2.4GHz, a  $\frac{1}{4}$  wavelength is approximately 3cm and at 5GHz, approximately 1.5 cm. In addition, the polarization of the radio signals can be altered as they passes through different mediums such as walls and doors. By placing the two antennas at 90° to each other maximises the likelihood that at least one of them will be correctly oriented to receive a strong signal. This is illustrated in the following diagram.



## 7.6 RF Layout Checklist

Parameter	Description	Hint
Impedance (Z)	50Ω (single-ended)	<ul style="list-style-type: none"> <li>No external termination required, on-chip termination resistor is implemented.</li> </ul>
Trace Routing	Routing method	<ul style="list-style-type: none"> <li>RF traces should be as short as possible.</li> <li>RF traces should be surrounded by a strong ground with many vias connected to the reference ground.</li> <li>RF traces should be straight and always on the 1<sup>st</sup> layer. Avoid changing layers and any vias.</li> </ul>
Ground Plane	must be ground referenced	<ul style="list-style-type: none"> <li>The reference ground for RF traces should be on the 2<sup>nd</sup> layer.</li> <li>The reference ground of RF traces should be complete planes, and preferably unbroken.</li> </ul>
Others	Other notifications	<ul style="list-style-type: none"> <li>Do not let any noisy traces run near or cross RF traces, e.g. data lines, clock signals, digital power and ground traces, etc.</li> <li>Matching devices should be as small as possible, e.g. 0201 is better than 0402.</li> </ul>

## 8 Power Rails

MT3620 requires a regulated 3.3V power supply, for example from a DC-DC converter, to convert whatever source voltage rail is used to 3.3V.

The MT3620 power management unit (PMU) contains an under-voltage lockout (UVLO) circuit, low drop-out regulators (LDOs), a highly efficient buck converter, a reference band-gap circuit and a voltage comparator for brown-out detection. These circuits are optimized for low quiescent current, low drop-out voltage, good line/load regulation, good ripple rejection and low output noise.

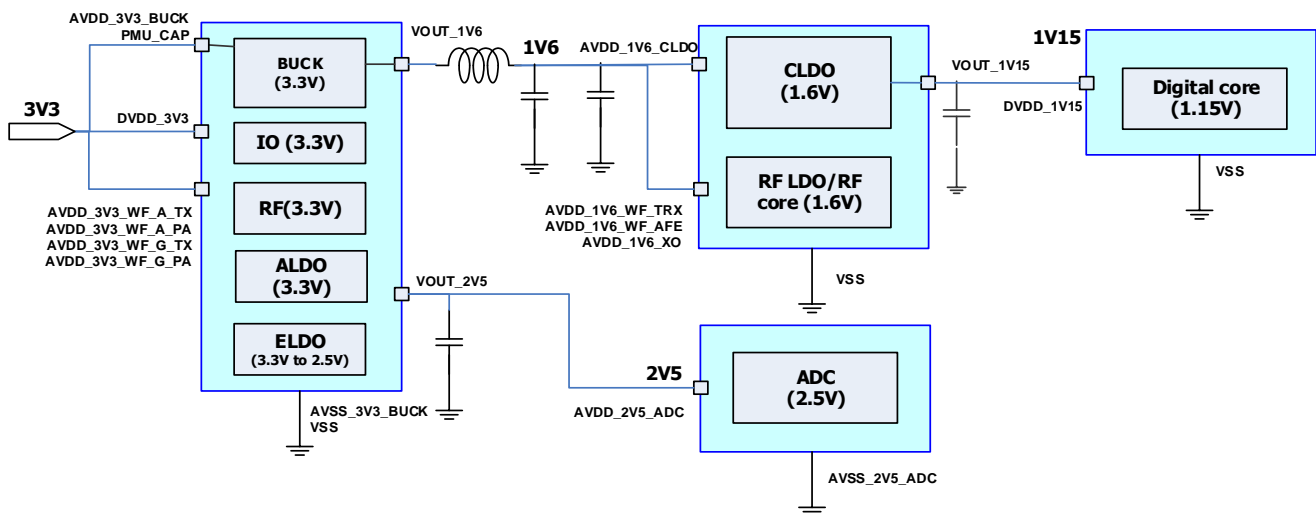
### 8.1 MT3620 PMU Architecture

The PMU integrates one buck converter and three LDOs: CLDO, ALDO, ELDO (CLDO: digital core LDO, ALDO: ADC LDO, ELDO: e-fuse LDO).

The buck DC-DC converter generates a 1.6V output to power other MT3620 sub-systems. Through an external LC filter (based on a 2.2uH inductor and a 10uF capacitor), it outputs a low ripple 1.6V for the Wi-Fi RF system, and CLDO. The CLDO generates 1.15V for the whole chip digital circuit from the 1.6V buck-converted domain.

For ADC requirements, the ALDO is integrated to generate 2.5V from the 3.3V chip supply. By default, the ALDO is off after power-on. It should be enabled before use and disabled it when not in use to save power.

The ELDO (e-fuse LDO) is also integrated into the PMU. It provides a 2.5V output voltage for the e-fuse logic and supports 60mA of maximum operation current. The ELDO is automatically and dynamically enabled and disabled by the e-fuse controller. It is not necessary to enable/disable it in software.



**Figure 8-1 Chip Power Block Diagram**

## 8.2 MT3620 Power Plan

Internally to the MT3620, the 3.3V power source is directly supplied to the switching regulator, digital I/Os and RF related circuitry. It's converted to 2.5V by the LDO for e-fuse and ADC analog circuitry, and it's converted to 1.6V by the switching regulator for low voltage circuits. The built-in digital LDOs and RF LDOs convert 1.6V to 1.15V for digital, RF, and BBPLL core circuits.

The following figure describes the MT3620 power tree.

**Table 8-1 MT3620 Power Rail Table**

Voltage	Source	Default State	Usage	Comment
3.3V	external power supply	--	PMU, IO , RTC and RF	*3 (both RTC 3.3v and the common 3.3v supply)
2.5V	ALDO	off	ADC analog macro	*3
2.5V	ELDO	off	e-fuse macro	*3
1.6V	Buck (normal mode/low power mode)	BUCK on	RF and XTAL	*3
1.15V	CLDO (normal mode/low power mode)	CLDO on	Digital core logic	*3

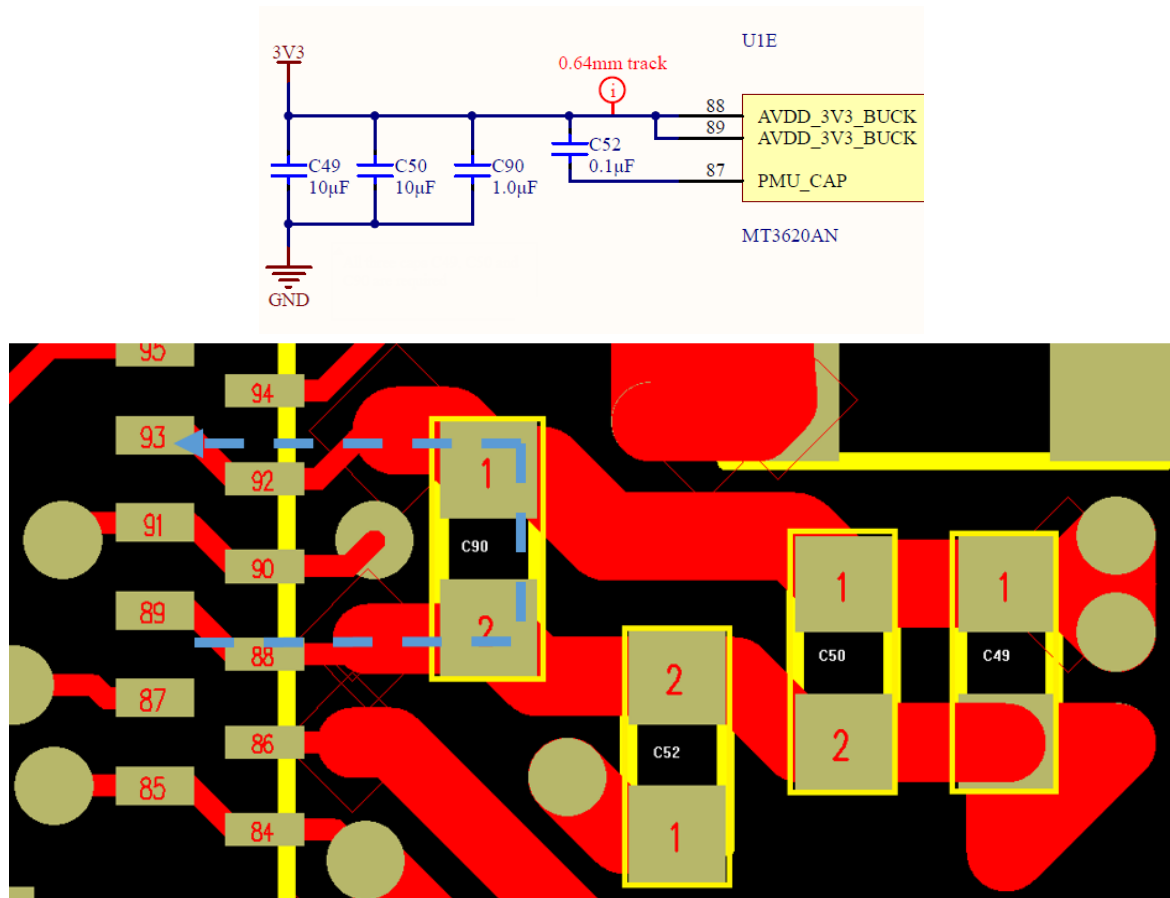
We strongly recommend using decoupling capacitors on each power rail.

### 8.2.1 PMU Buck 3.3V Supply Input

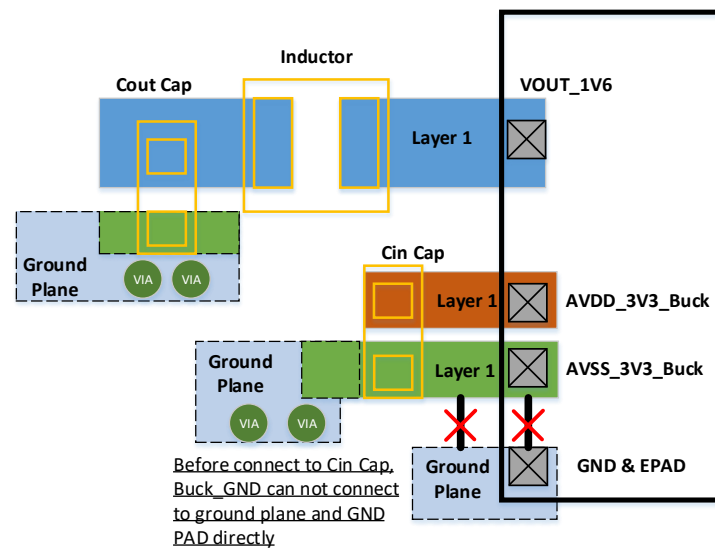
Several items are noticed here,

For 3.3V source recommend specifications

1. AC+DC 3.3V  $\pm 10\%$  (2.97V~3.63V)
  2. PWM Ripple < 10 mVpk-pk @ 1.1A
  3. Load Transient Drop and overshoot  $\pm 100\text{mV}$  @3.3V  $I_{\text{out}}=0$  to 1.1A
  4.  $I_{\text{max}} \geq 1.1\text{A}$  (For Buck and LDO Inrush current)
- 0.1uF capacitor (C52) should be close to Pin AVDD\_3V3\_BUCK(88,89) and PMU\_CAP(87). 10uF capacitors (C49,C50) are behind 1uF (C90) and close to AVDD\_3V3\_BUCK (88,89) as following Figure 8-2. The trace width from 3.3V power source to chipset (AVDD\_3V3\_BUCK pins) should be  $\geq 0.64\text{mm}$ . AVSS\_3V3\_BUCK (92,93) should wire 0.64mm least trace to C49 and C50 GND pin first, then vias to ground plane.
  - PCB constrain "C90 to pin 88/89 PCB parasitic L + C90 to pin 92/93 PCB parasitic L" < 1.5 nH  
This is for reliability to protect large bonding inductance in package.



**Figure 8-2 PMU Buck Circuit and Layout Placement**



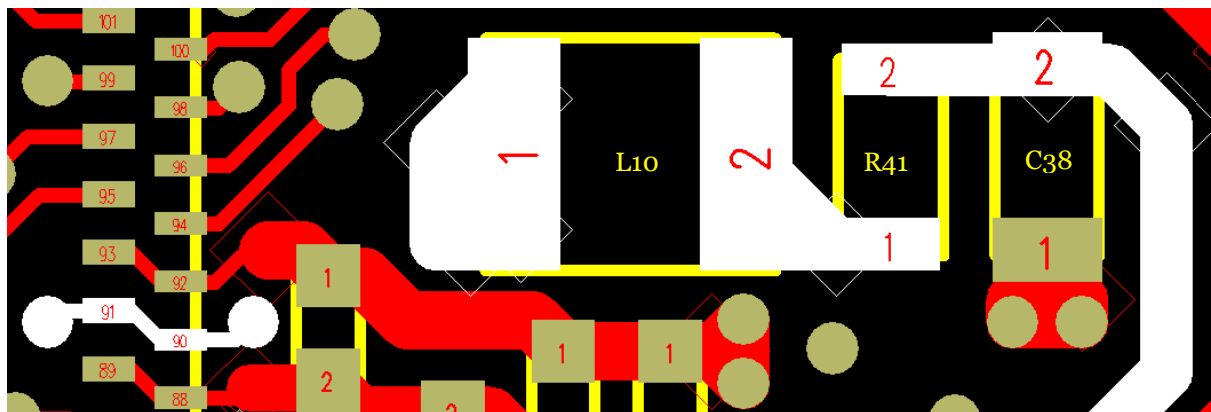
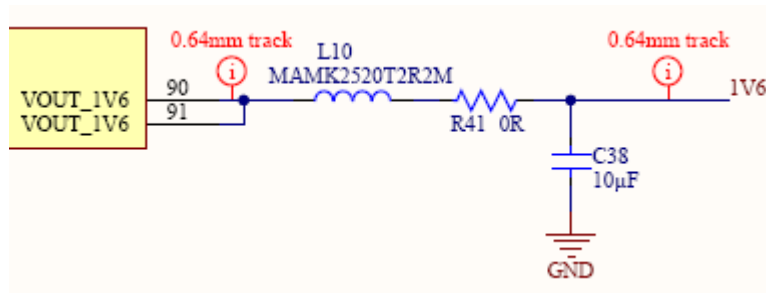
**Figure 8-3 PMU Buck Ground Layout**

### 8.2.2 PMU Buck 1.6V Supply Output

Several items should be noticed here:

The inductor L10 should be placed as closely as possible to the VOUT\_1V6 pins (90, 91) and the 10uF capacitor C38 should be close to L10 as shown in Figure 8-4.

- The trace width from VOUT\_1V6 to C38 should be at least 0.64mm.
- The total recommend capacitance is: 10uF+1uF near VOUT\_1V6; and three 2.2uF capacitors far from VOUT\_1V6.



**Figure 8-4 PMU VOUT\_1V6 Circuit and Layout Placement**

MTK requires the power inductor should meet:

- The inductance value is 2.2uH
- The inductance decrease is <30% if the loading current on inductor increases to 1.4A.
- The typical DC resistance of the inductor is less than 100m ohm.

According to above requirements, the power inductor MTK recommended is in following table.



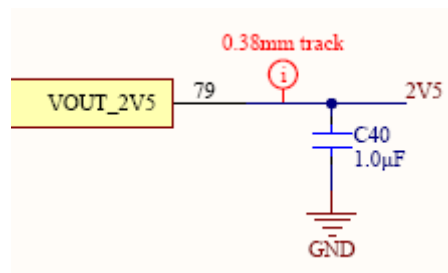
**Table 8-2 Power Inductor QVL list**

Component	Part Number	Manufacturer	Vendor	Size(mm)	Status	Temp. (°C)
Power inductor	CIGT252010LM2R2MNE	Samsung	Samsung	2520	Approved	-10~ +70
Power inductor	CIGT252012LM2R2MNE	Samsung	Samsung	2520	Approved	-10~ +70
Power inductor	MAMK2520T2R2M	Taiyo	Taiyo	2520	Approved	-10~ +70

### 8.2.3 PMU LDO 2.5V Supply Output

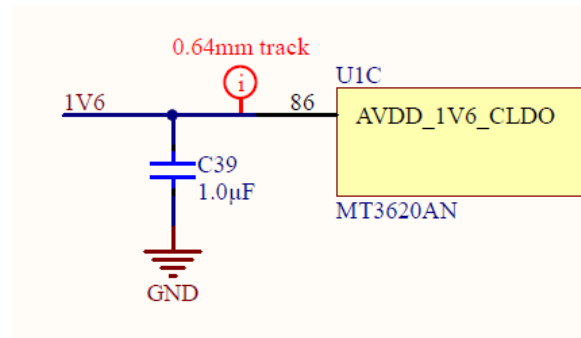
Several items should be noticed here:

- The trace width between 1uF and VOUT\_2V5 pin (79) should be  $\geq 0.38\text{mm}$ .
- Total capacitance recommend on 2.5V power rails: 2uF (near MT3620: 1uF, near usage : 1uF)
- PCB trace parasitic resistance and inductance recommended to be below
  - Trace define from VOUT\_2V5 to C40
  - Trace resistance < 40 mohm
  - Trace inductance < 2nH


**Figure 8-5 PMU VOUT\_2V5 Output Circuit**

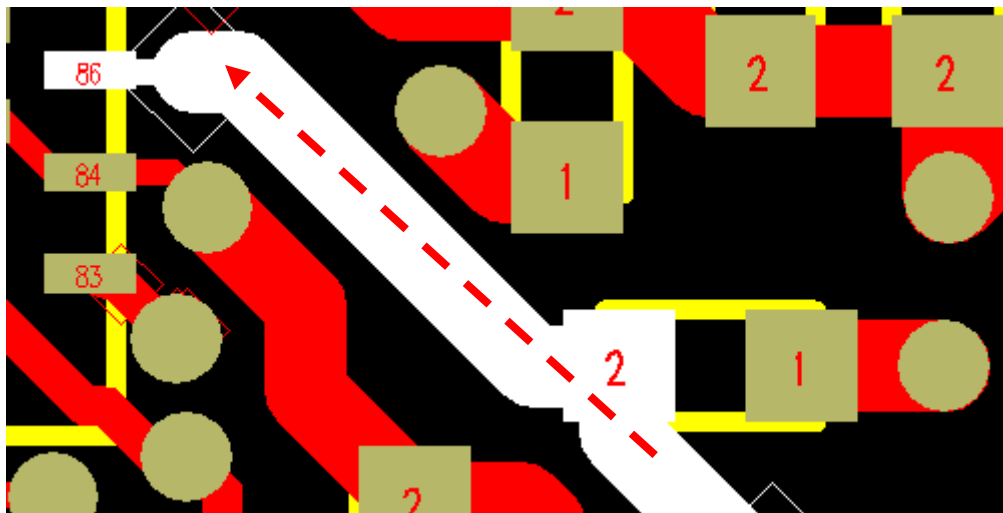
### 8.2.4 PMU LDO 1.6V Supply Input

- A 1uF decoupling capacitor should be close as possible to AVDD\_1V6\_CLDO (86) following Figure 8-6 and the trace width between this 1uF capacitor and pin AVDD\_1V6\_CLDO should be  $\geq 0.64\text{mm}$ .



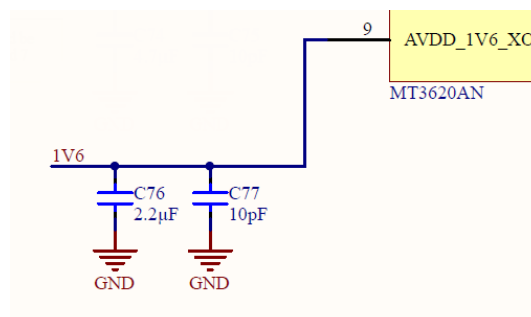
**Figure 8-6 PMU 1.6V LDO Input Circuit**

- Since buck feedback sense AVDD\_1V6\_CLDO that need to prevent noise couple to buck feedback, AVDD\_1V6\_CLDO trace should keep away from switching noise. (Figure8-7)



**Figure 8-7 AVDD\_1V6\_CLDO Input Layout**

- AVDD\_1V6\_XO (9) should have 10pF and 2.2µF decoupling capacitors as per following figure. In addition, a 0 ohm series resistor footprint can be included in front of C76 and C77 if it becomes necessary to reduce noise.

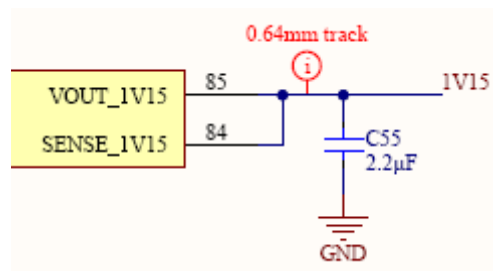


**Figure 8-8 RF AVDD\_1V6\_XO Input Circuit**

## 8.2.5 PMU LDO 1.15V Supply Output

Several items should be noticed here:

- VOUT\_1V15 and SENSE\_1V15 share a single 2.2uF decoupling capacitor.
- The trace width between 2.2uF and VOUT\_1V15 pins (84,85) should be  $\geq 0.64\text{mm}$ .
- Total recommend capacitance is 2.2uF~6.5uF (near PMU=2.2uF, near point of use=0~4.3uF) while using internal 1.15V VCORE PMU.
- PCB trace parasitic inductance and resistance are recommended as follows:
  - Trace define from VOUT\_1V15 to C55.
  - Trace Resistance  $< 20\text{ mohm}$ .
  - Trace Inductance  $< 2\text{nH}$ .



**Figure 8-9 VOUT\_1V15 LDO Output Circuit**

- A 0.1uF capacitor should be fitted close to each DVDD\_3V3 power pin
- A 0.47uF capacitor should be fitted close to each DVDD\_1V15 power pin. In the case of pins 77 and 78, a single 0.1uF capacitor may be used instead of two 0.47uF capacitors. A maximum of 4.3uF closely-located decoupling is recommended for DVDD\_1V15.
- Decoupling capacitors can be connected with a return path through the e-pad if that is more convenient than using GND pins.

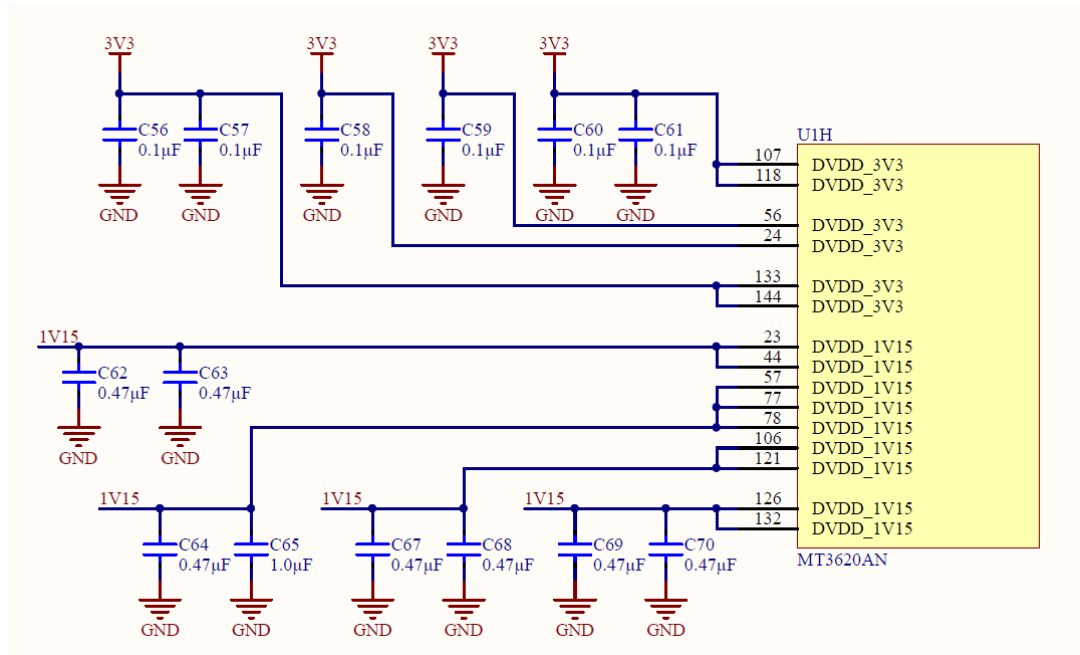


Figure 8-10 DVDD\_3V3 and DVDD\_1V15 Power Circuit

### 8.3 RTC Battery Supply

The RTC requires an external battery connection to maintain its functionality while the MT3620 is not powered by the system. And battery type is CR2032, which can give many years of operation. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170mAh (assumed usable) and the average current required is 5  $\mu$ A, the battery life will be at least:

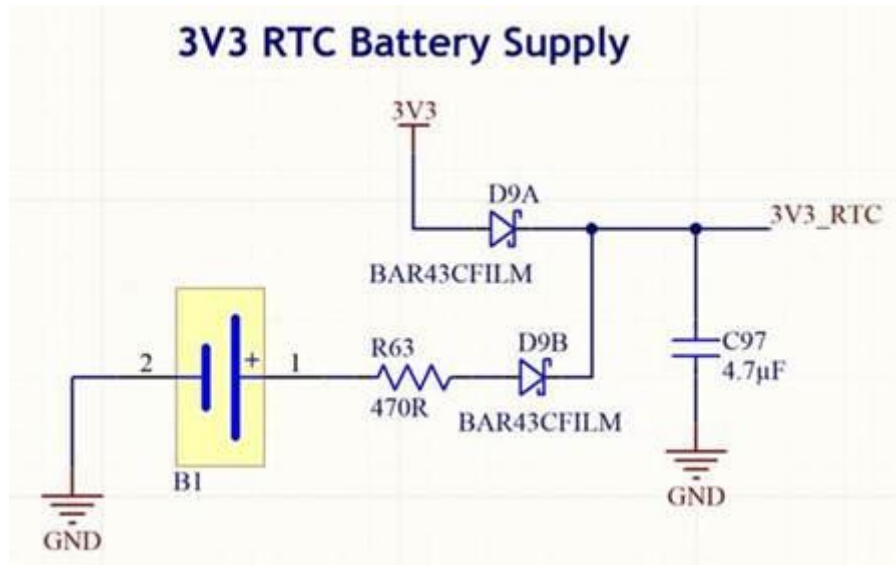
$$170,000 \mu\text{Ah} / 5 \mu\text{A} = 34,000 \text{ h} = 3.9 \text{ years}$$

The battery must be connected to the MT3620 via a Schottky diode circuit for isolation. The Schottky diode circuit allows the MT3620 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reversed biased when the system power is not available. A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy. Figure 8-11 is an example of a diode circuit that is used.

If strapping pins are configured to use an external 32 KHz crystal, 3V3\_RTC **must** be powered or the system will not start.

The above can be achieved by permanently connecting 3V3\_RTC to 3V3. However, for applications that require RTC operation even when the main 3.3V system power is removed, a backup power source is required. Depending on the application, the backup power source may be a primary cell, secondary cell, or super capacitor.

One common backup power source used in many devices is a primary cell battery (e.g. a CR2032 coin cell). In order to ensure system availability when using such a battery, designers should take care to use a circuit that allows the 3V3\_RTC to be sourced from either the battery or 3V3 system power. One possible circuit is shown in Figure 8-11, which is explained below. The circuit guarantees that even if the battery becomes depleted, the system will continue to start up if main system power is available. The circuit has the added benefit of minimizing power draw on the battery when system power is available, extending battery life.



**Figure 8-11 Battery and 3V3 Power Circuit for AVDD33\_RTC**

Several items should be noticed here:

- When the main 3V3 supply is present, D9B prevents the main supply from charging the battery.
- D9A prevents the battery from powering other parts of the system that are connected to the main 3V3 supply when operating from the battery alone.
- BAR43 Schottky diodes have a low forward voltage drop which is advantageous in this application, since it helps maximize the useful operating life of the battery.
- Lithium based primary coin cells can tolerate a small charging current, up to certain limits, without adversely affecting their operating life. Therefore, the reverse leakage current of the diodes should also be taken into consideration, particularly if the system will be operating in a hot environment ( $>50^{\circ}\text{C}$ ), since the reverse leakage current is proportional to temperature.
- R63 is included to limit the charging current to a safe level in the event D9B fails closed-circuit.

- The 4.7uF cap provides additional smoothing when switching between battery and main 3V3 (there is also a 100nF capacitor on the 3V3\_RCT line (not shown above), located close to the MT3620)

## 8.4 Power/GND Checklist

Table 8-3 specifies the checklist and guidelines for power and GND routing.

**Table 8-3. Checklist for Power and GND Routing**

Item	Type	Description	Ref section
[1] Power Capacitor Design guideline			
1-1	Suggestion	A decoupling capacitor (0.1uF) is suggested for each power pin.	N/A
1-2	Mandatory	Decoupling capacitors (0.1uF) must be placed as close as possible to power pins.	N/A
1-3	Mandatory	Decoupling capacitors (0.1uF) must have a low loop inductance.	N/A
1-4	Mandatory	Larger decoupling capacitors (10uF, 2.2uF, 1uF) must be placed as close as possible beside the relevant power pins.	N/A
1-5	Mandatory	Larger decoupling capacitors (10uF, 2.2uF, 1uF) is required power shape with multi-vias or high current Via for power\GND.	N/A
1-6	Mandatory	Buck 3.3V input parasitic from pin to capacitor need to meet 1.5nH spec. “The inductance of C90 to AVDD_3V3_BUCK + The inductance of C90 to AVSS_3V3_BUCK”<1.5nH Buck input capacitor should be close to the IC to reduce parasitic inductance.	4.2.1

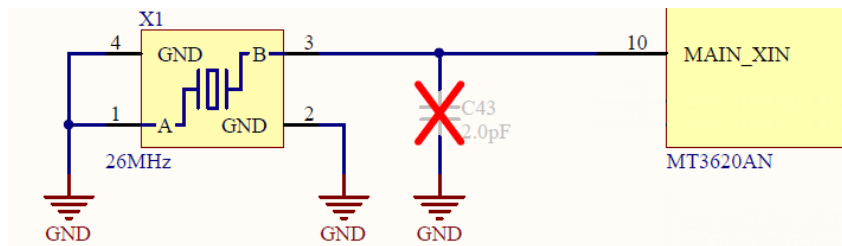
## 9 Clock

Table 5-1 below shows the specification of crystal components. MTK strongly recommends following this table when selecting a crystal for MT3620.

**Table 9-1. Recommend 26MHz XTAL Spec for MT3620**

Parameter	Specification
Frequency Tolerance@25 °C	±10ppm
Frequency Stability over temperature	±10ppm
ESR	<= 30ohm
CL	10.5p~12.0p
TS	>= 10ppm/pF
DL	>= 100uW
Dimension	3225 or 2520

The MAIN\_XIN pin must be connected to an external 26MHz crystal as shown in Figure 9-1. The recommended value of CL and Rd are shown in Table 9-2.



**Figure 9-1 XTAL Circuit**

**Table 9-2. Recommend Rd/CL Value of XTAL Circuit**

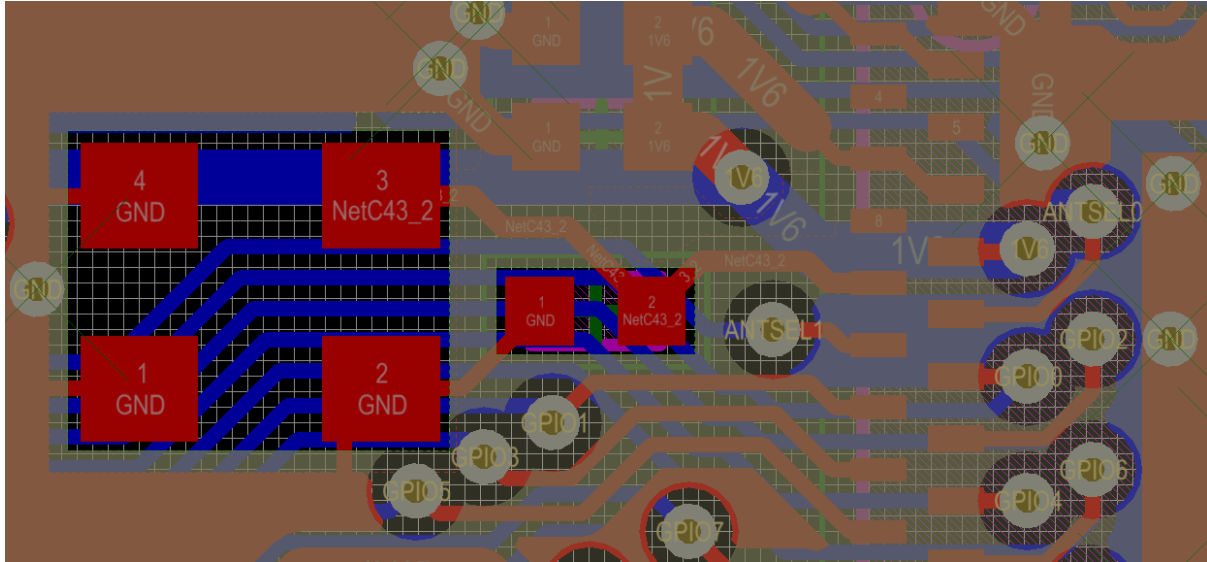
Parameter	Description	Hint
XTAL	- CL = 10.5pF	- Need consider the PCB trace capacitance loading.
	- Rd: 0 ohm	- Reserved Rd resistance with mounted oohm.
Trace Loading	- <1pF	- PCB trace will contribution capacitance loading - 7mil width and 300mil length trace capacitance is about 1pF

These values are given only as a typical example and considered the 300mil length of PCB trace capacitance effect. Please refer to the crystal datasheet to determine the correct capacitor value.

### 9.1 XTAL Routing Guide

Guidelines relating to crystal layout are given below.

- The components on the crystal path need a keep-out anti-pad on layers 1 and 2, with the ground reference being layer 3.
- The clock trace running outside the keep-out area needs to have a 50ohm impedance in relation to layer 2.
- The clock trace should be as short as possible with a total trace loading of <1pF.



**Figure 9-2. Crystal Layout Placement and Routing, Showing Layer 2 Keep-out**

Layout guidelines for the single-ended clock are given in Table 9-3.

**Table 9-3. Clock Routing and Layout Guidelines**

Parameter	Description	Hint
Impedance(Z)	- 50Ω (single-end)	- No external termination required, on-chip Termination resistor is implemented.
Via qty	- 0	- Recommended. - Single trace from end to end.
Keep out	- Far away high speed signal. - Far away the edge of the plane.	- Do not route clock traces under high speed signals. - Route all clock traces over continuous planes, with no interruptions. Avoid crossing over anti-etch if at all possible.
Anti-Pad	- Layer-1, Layer-2	- Recommended.



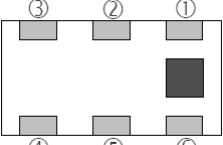
		<ul style="list-style-type: none"> <li>- Remove crystal, resistor, capacitor pad area on layers 1 and 3, use layer 3 as a ground reference.</li> </ul>
Ground Plane	- must be ground referenced.	<ul style="list-style-type: none"> <li>- Clock signals must be ground referenced and shielded.</li> <li>- Unbroken ground plane are preferred.</li> <li>- Route all traces over continuous planes, (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible</li> </ul>

## 10 Critical Components

### 10.1 Critical RF Components

#### 10.1.1 Balun

- The Balun is a monolithic SMD with small, low-profile and light-weight type.
- The dimension of balun is 1.6 x 0.8 mm<sup>2</sup> which is known 1608 type.
- The impedance of balanced and unbalanced ports are both 50Ω
- The balun specifications MTK recommend are in following tables.

	No.	Pin Definition	No.	Pin Definition
	1	Unbalanced Port	4	Balanced Port
	2	GND or DC feed + RF GND	5	GND
	3	Balanced Port	6	NC

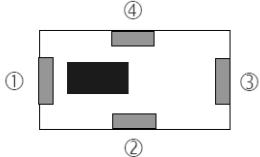
Parameter	MTK Spec.	Min	Typ.	Max.	Unit
Port Impedance	Balance Port impedance		50		Ohm
	Unbalance Port impedance		50		Ohm
Frequency Range	Frequency Range	2400		2500	MHz
Target Spec	Insertion Loss		0.8	0.88	dB
	VSWR			2.0	
	Phase Difference	170	180	190	degree
	Amplitude Difference			2	dB

#### Qualified balun list:

Component	Part Number	Manufacturer	Size (mm <sup>2</sup> )	Status	Temp. (C)
2.4G Balun	BL1608-05A2450TB	ACX	1608	Approval	-10~ +70
2.4G Balun	RFBLN1608050AM8T62	Walsin	1608	Approval	-10~ +70

### 10.1.2 Diplexer

- The dimension of diplexer is 1608 type which should have enough out-of-band rejection to attenuate 2<sup>nd</sup> harmonic and VCO leakage of 2.4GHz and 5GHz signals.
- The diplexer MTK recommends should have electrical characteristics as per the following table.

	No.	Pin Definition	No.	Pin Definition
	1	Low Band Port	3	High Band Port
	2	Common Port	4	GND

Parameter	MTK Spec.	Min	Typ.	Max.	Unit
Port Impedance	Low Band Port impedance		50		Ohm
	High Band Port impedance		50		Ohm
	ANT Port		50		Ohm
Passband Frequency Range	Low Band Port	2400		2500	MHz
	High Band Port	4900		5950	MHz
Insertion Loss	Low Band Port			0.8	dB
	High Band Port			0.9	dB
<b>Low Band Port</b>					
Attenuation	4800 – 6000MHz	20			dB
	7200 – 7500MHz	20			dB
<b>High Band Port</b>					
Attenuation	1800 – 2500MHz	20			dB
	3600 – 3900MHz	10			dB
	9800 – 11900MHz	20			dB

#### Qualified Diplexer list:

Component	Part Number	Manufacturer	Size (mm <sup>2</sup> )	Status	Temp. (C)
2.4/5GHz DPX	DP1608-A2455SC	ACX	1608	Approval	-10~+70
2.4/5GHz DPX	DPX165950DT-8018A1	TDK	1608	Approval	-10~+70

## 11 Boot Strapping Pins

Immediately after coming out of reset, the MT3620 senses the state of a number of ‘strapping’ pins to configure various internal sub-systems of the chip. The following table provides details of which pins are used for strapping, along with their function and default state. In all cases, strapping pins should be pulled high or low through 4.7K resistors.

Function	Pin	Default	Notes
Reserved	DEBUG_TXD	Pull low	Must be pulled low
RTC clock	RECOVERY_TXD	Pull high	Pull high for ext. 32kHz crystal Pull low for internal 32kHz clock
Crystal frequency	IO0_RTS	Pull high	Must use this configuration for 26MHz crystal
	IO0_TXD	Pull low	
Reserved	IO1_TXD	Pull low	Must be pulled low
Reserved	RECOVERY_RTS	Pull low	Must be pulled low
Recovery mode	DEBUG_RTS	Pull low	Pull low for normal mode Pull high for recovery mode

## 12 SMT Guidelines

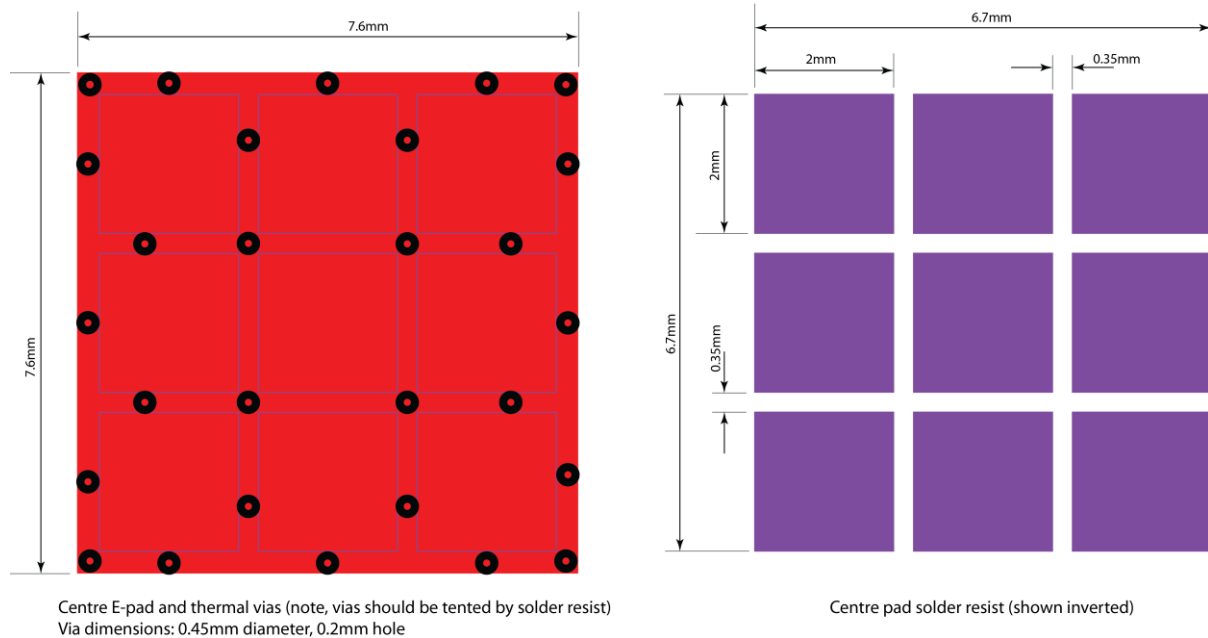
### 12.1 Recommended Pad Specification

The via size, width and the distance between via and trace are list as below

via size	$a1/a2$	0.2mm (finished hole) / 0.45 mm (copper diameter)
trace width	$b$	0.125 mm
via to via	$x$	0.575 mm
via to trace	$y$	0.125 mm
trace to trace	$z$	0.125 mm

## 12.2 E-pad PCB Footprint

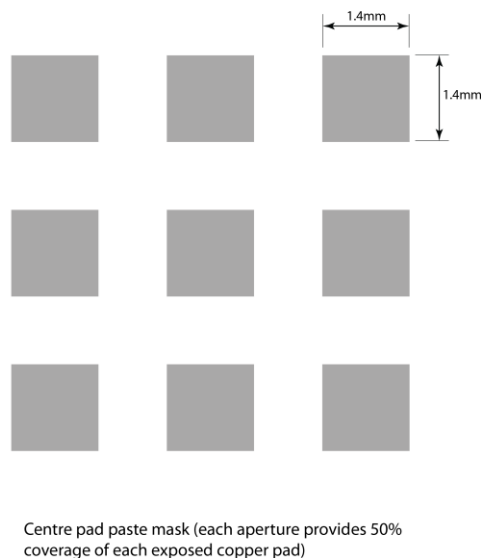
The following diagram provides details of the recommended E-pad PCB footprint:



**Figure 11-12-1. Recommended E-pad PCB footprint**

## 12.3 E-PAD Soldering Guideline

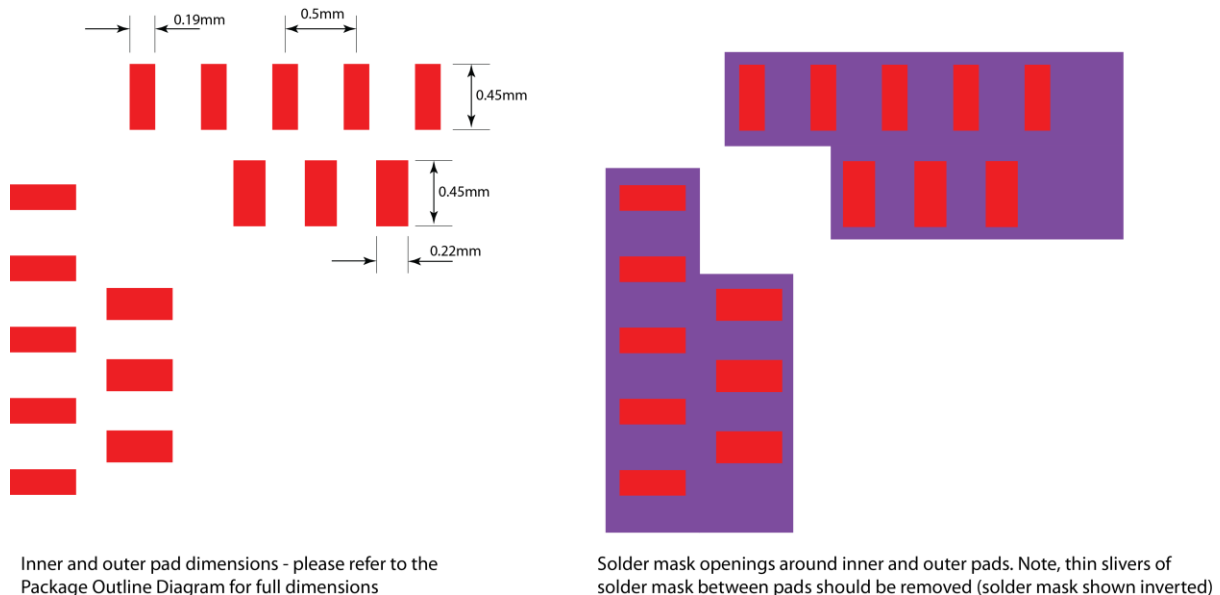
The following diagram provides details of the solder stencil openings for the E-pad:



**Figure 11-12-2. Recommended E-pad solder paste stencil**

## 12.4 Signal Pad PCB Footprint

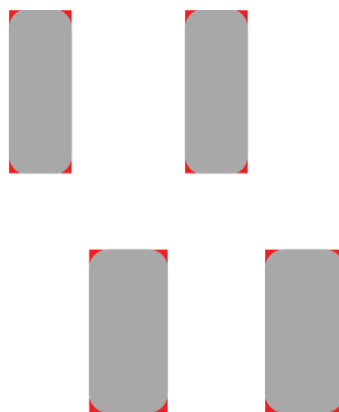
The following diagram provides details of the recommended signal pad PCB footprint:



**Figure 11-12-3. Recommended signal pad PCB footprint**

## 12.5 Signal Pad Soldering Guideline

The following diagram provides details of the solder stencil openings for the signal pads:



**Figure 11-12-4. Recommended signal pad solder paste stencil**

## 12.6 Reflow Profile Guideline

The following reflow profile guideline is designed for SnAgCu lead-free solder paste. MTK recommend that customers follow their specific solder paste vendor's guideline and design a profile appropriate to their line and product. An appropriate N<sub>2</sub> atmosphere is recommended since it will widen the process window and mitigate the risk of soldering issues.

